UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,923	03/10/2004	Shoichi Furuhata	FUJI:300	3352

37013 7590 04/21/2005

ROSSI & ASSOCIATES
P.O. BOX 826
ASHBURN, VA 20146-0826

EXAMINER	
DICKEY, THOMAS L	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 04/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/797,923	FURUHATA, SHOICHI	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *10-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7 and 8* is/are rejected.

7)☒ Claim(s) *6 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/10/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

1. Applicant's election of Group II, claims 1-9 in the Paper filed 03/31/2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Oath/Declaration

2. The oath/declaration filed on 03/10/2004 is acceptable.

Drawings

3. The formal drawings filed on 03/10/2004 are acceptable.

Priority

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

5. The Information Disclosure Statement filed on 03/10/2004 has been considered.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5,7, and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by BOSSELAAR ET AL. (4,148,053).

With regard to claims 1-3, Bosselaar et al. discloses a semiconductor wafer comprising a first conduction type low concentration impurity layer 1 formed beneath a principal face of a wafer to a predetermined depth; a first conduction type high concentration impurity layer 2 having an impurity concentration (note column 4 lines 19-20) of 5X1019/cc (and thus, inherently, resistance value not higher than 0.05 Ω•cm, note figure 6 of Kroger 4,544,937) underlying said low concentration impurity layer 1; and a first conduction type high concentration impurity diffusion region 6 having a lattice-shaped pattern (Note figure 2 of

Rowe 4,040,878, which is incorporated by reference into Bosselaar et al. at column 4 line 60), formed along at least a portion of the dicing lines A-A that delimit a plurality of chips (again, the plurality of chips is seen most clearly in figure 2 of Rowe 4,040,878, which is incorporated by reference into Bosselaar et al.) on said wafer, said diffusion region 6 extending from the principal face of the wafer to said high concentration impurity layer 2, wherein said diffusion region 6 has a width larger than that of the cutting allowance for the dicing along the dicing lines A-A. Note figures 4-6, column 4 lines 19, 20, and 49-64, column 5 lines 56-60, and column 6 lines 35-39 of Bosselaar et al.

With regard to claims 4, 5, 7, and 8, Bosselaar et al. discloses a semiconductor wafer comprising a first conduction type low concentration impurity layer 1, a first conduction type high concentration impurity layer 2 having an impurity concentration (note column 4 lines 19-20) of 5X1019/cc (and thus, inherently, resistance value not higher than 0.05 Ω•cm, note figure 6 of Kroger 4,544,937) underlying said low concentration impurity layer 1, and a first conduction type high concentration impurity diffusion region 6 that extends from the upper surface of said low concentration impurity layer 1 to said high concentration impurity layer 2, said diffusion region 6 being positioned at the outer edge of an element region 3 having a semiconductor element 4 formed therein, wherein said diffusion region 6 comprises a

portion or the entirety of dicing regions A-A on a wafer containing said device, wherein said high concentration impurity diffusion region 6 electrically connects said high concentration impurity layer 2 with at least one electrode 35 positioned above said low concentration impurity layer 1, by being electrically connected with at least one electrode 35 formed on the upper surface of said low concentration impurity layer 1. Note figures 4-6, column 4 lines 19, 20, and 49-64, column 5 lines 56-60, and column 6 lines 35-39 of Bosselaar et al.

Allowable Subject Matter

7. Claims 6 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thomas L. Dickey
Patent Examiner
Art Unit 2826
04/05